AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-14 (canceled)

15. (new) A data processor comprising an instruction unit, which includes:

an instruction register having two parts each of n-bit length;

a register conflict detection circuit; and

an instruction decoder adapted to decode first instructions having n-bit length and second instructions having 2n-bit length,

wherein the instruction register fetches instruction data of 2n-bit length and having at least one instruction,

wherein the two parts of the instruction register are capable of providing register information, from a same location in each of the two parts of the instruction register, to the register conflict detection circuit for detecting a register conflict;

wherein the register conflict detection circuit uses register information from both of the two parts of the

instruction register for detecting register conflict when both parts contain first instructions and when a first of the two parts contains a first instruction and a second of the two parts contains a first n-bit portion of a second instruction, and

wherein the register conflict detection circuit uses register information from only one of the two parts of the instruction register for detecting register conflict when the first part contains a first instruction and the second part contains a second n-bit portion of a second instruction, and when the instruction register contains one second instruction.

16. (new) A data processor according to claim 15,

wherein when said register conflict detection circuit detects a register conflict in accordance with the register information provided from each of the two parts of the instruction register, the register conflict detection circuit provides a conflict signal, and

wherein the instruction unit controls execution of instructions in accordance with the conflict signal.

17. (new) A data processor according to claim 15,

wherein each said second instruction includes a register information field in a first n-bit portion thereof.

18. (new) A data processor according to claim 15,

wherein the instruction decoder is adapted to decode third instructions having 2n-bit length,

wherein the first instructions, the second instructions, and the third instructions include first register information in a first n-bit portion of instruction data, and the third instructions further include second register information of a second n-bit portion of instruction data following the first n-bit portion thereof, the first register information and the second register information being at the same location in the respective portions of instruction data;

wherein when the second n-bit portion of a second instruction is stored into one of the two parts of the instruction register, the register conflict detection circuit does not use the register information provided from the one of two parts of the instruction register in response to the result of decoding instruction by the instruction decoder, and

wherein when the second n-bit portion of a third instruction is stored into one of two parts of the

instruction register, the register conflict detection circuit uses the register information provided from the one of two parts of the instruction register in response to the result of decoding instruction by the instruction decoder.